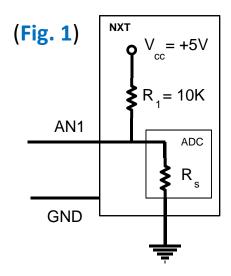
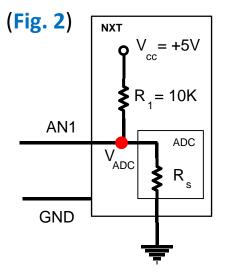
Voltage Dividers and the NXT





 R_1 is called a pull-up resistor. It's built into the NXT (for circuit protection). Not known, is R_s which represents the impedance (resistance) due the NXT's ADC.

As drawn (with no inputs on AN1), the ADC will read HI (i.e. close to 5V). Actually, the real value will depend on R_s since there is a voltage divider.

$$I = \frac{V_{cc}}{R_1 + R_s}$$
 and $I = \frac{V_{ADC}}{R_s}$

Thus have: $\frac{V_{cc}}{R_1 + R_s} = \frac{V_{ADC}}{R_s}$ and hence $V_{ADC} = \frac{R_s}{R_1 + R_s} V_{cc}$

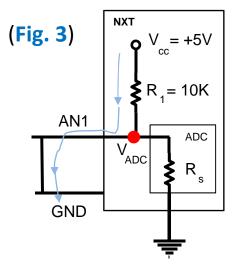
RS [Ohm]	R1 [Ohm]	VCC [V]	VADC [V]	I [A]	I [mA]
100	10000	5	0.05	4.95E-04	0.50
250	10000	5	0.12	4.88E-04	0.49
500	10000	5	0.24	4.76E-04	0.48
1000	10000	5	0.45	4.55E-04	0.45
1500	10000	5	0.65	4.35E-04	0.43
2500	10000	5	1.00	4.00E-04	0.40
5000	10000	5	1.67	3.33E-04	0.33
7500	10000	5	2.14	2.86E-04	0.29
10000	10000	5	2.50	2.50E-04	0.25
20000	10000	5	3.33	1.67E-04	0.17
50000	10000	5	4.17	8.33E-05	0.08
100000	10000	5	4.55	4.55E-05	0.05
150000	10000	5	4.69	3.13E-05	0.03
200000	10000	5	4.76	2.38E-05	0.02
500000	10000	5	4.90	9.80E-06	0.01
1000000	10000	5	4.95	4.95E-06	0.00

One observes that:

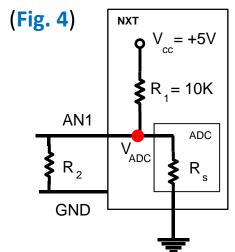
 $R_{\it S}$ small, then $V_{\it ADC}$ small

 $R_{\scriptscriptstyle S} > 100 k \Omega$, then $V_{\scriptscriptstyle ADC} \to 5 V$

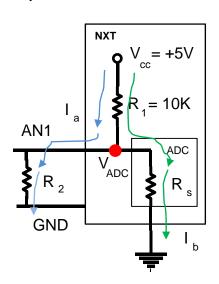
So maybe ADC impedance is quite high?



Lets short AN1 and GND e.g. by closing a switch. The path of least resistance is depicted in blue. Here, the ADC should read 0 Volts, or $V_{ADC}=0$ V. Thru my switching experiments, I've verified that this is true. Also, imagine all the current will flow thru the switch (i.e. short). The value is $I = \frac{V_{cc}}{R_1} = \frac{5 V}{10000 \Omega} = 0.00005 A = 0.5 mA$



If insert resistor R_2 across AN1 and GND, we actually have a parallel resistor network due to R_2 and R_s



$$I = I_a + I_b = \frac{V_{cc}}{R_1 + R_2} + \frac{V_{cc}}{R_1 + R_s}$$

Thus, if R_s is high, then current from V_{cc} will like to mostly flow thru R_2

Suppose say:

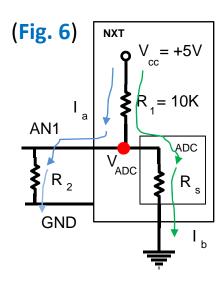
 $R_s \triangleq 100k\Omega$ (guessing a high value)

$$R_2 \coloneqq 220\Omega$$

$$I_a = \frac{5}{10000 + 220} = 0.49 \, mA$$

and

$$I_b = \frac{5}{10000 + 100000} = 0.045 \, mA \tag{1}$$



If insert resistor R_2 across AN1 and GND, we actually have a parallel resistor network due to R_2 and R_s

$$\frac{1}{R_T} = \frac{1}{R_2} + \frac{1}{R_S} = \frac{R_S + R_2}{R_2 R_S}$$
 or $R_T = \frac{R_2 R_S}{R_S + R_2}$

 V_{ADC} is now the voltage drop across the parallel resistor network

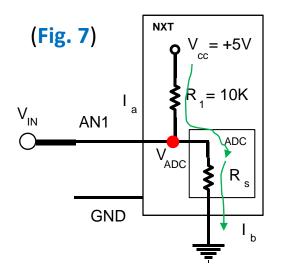
$$V_{ADC} = \frac{R_T}{R_1 + R_T} V_{cc}$$

Suppose say: $R_S \triangleq 100k\Omega$ and $R_2 \coloneqq 220\Omega$ Hence: $R_T = \frac{220 \cdot 100000}{220 + 100000} = 219.5 \Omega$

Calculating V_{ADC} we have

$$V_{ADC} = \frac{219.5}{10000 + 219.5} \, 5 = 0.11 \, V$$

In other words, R_2 serves as a pull-down resistor. It forces (most of the) current from V_{cc} to flow thru R_2 . Also, the (voltage) contribution due to V_{cc} will be a little (0.11 Volts).

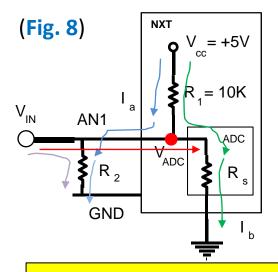


Now suppose there's a voltage input V_{IN} . Perhaps it's from a temperature sensor like the LM35. Suppose that the voltage is very small, say $10\ mV$ to $1\ V$...

In other words, $V_{IN} \ll V_{cc}$. From Fig. 1, we again see that V_{ADC} will be dominated by V_{cc} .

Furthermore, current into the ADC will be mainly due to V_{cc} , flowing thru R_1 and R_s .

For this reason, one cannot simply attach a low-voltage device like the LM35 into AN1. The NXT's internal +5 Volt supply overpowers the LM35's low-voltage.

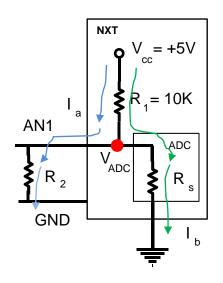


From Fig. 6, we see that adding R_2 across AN1 and GND, is called a pull-down resistor; it forces the current from V_{cc} to flow into R_2 and contributes very little (0.11 V) to V_{ADC} . From (1) we calculated the current I_b is also very small (0.045 mA).

The ADC will just (mainly) be V_{IN} (which is what we want). The current from V_{IN} will mainly go thru R_2 but that's OK.

QED: Putting a pull-down resistor R_2 (220 Ω) solves the problem; it allows one to hook up low-voltage sensors like the LM35, directly into AN1



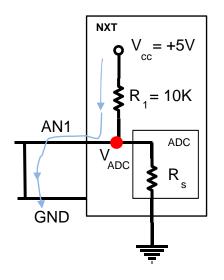


$$R_T = \frac{R_2 R_S}{R_S + R_2}$$

The current I flows thru both R_2 and R_s . Let $I=I_a+I_b$

$$I = \frac{V_{ee}}{R_1 + R_T} = \frac{V_{ee}}{R_1 + \frac{R_2 R_s}{R_s + R_2}} = \frac{V_{ee}}{\frac{R_1 (R_s + R_2) + R_2 R_s}{R_s + R_2}}$$

$$I_a = \frac{V_{cc}}{R_1 + R_2}$$
 and $I_b = \frac{V_{cc}}{R_1 + R_s}$ Hence $I = I_a + I_b = \frac{V_{cc}}{R_1 + R_2} + \frac{V_{cc}}{R_1 + R_s}$



Lets short AN1 and GND e.g. by closing a switch. The path of least resistance is depicted in blue. Here, the ADC should read 0 Volts, or $V_{ADC} = 0 \ V$. Thru my switching experiments, I've verified that this is true.

Also, I imagine all the current will flow thru the switch (i.e. short). The value is $I = \frac{V_{cc}}{R_1} = \frac{5 V}{10000 \,\Omega} = 0.00005 \, A = 0.5 \, mA$

Blah: What's the NXT's ADC micro? EG: Atmel? What's the current limits?

NXT Processor: Atmel 32-bit AT91SAM7S256. One 8-channel 10-bit ADC. Pg. 574 (of 775 PDF) says that the Input Leakage Current is typically 1 uA

Suppose $R_{\rm S}=100k\Omega$ (i.e. something high) and $R_2\ll R_{\rm S}$. Then can see that current will prefer to flow through R_2 .

